

INTRASERVER TAG-SWITCHED DISTRIBUTED  
PACKET PROCESSING FOR NETWORK ACCESS SERVERS

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ABSTRACT OF THE DISCLOSURE

An access server architecture, and methods for use of the architecture, are disclosed. The architecture and methods are designed to increase the scalability of and balance processor load for a network access server device. In this architecture, packet forwarding and packet processing are distributed amongst the cards serving the  
10 low-speed access lines (i.e., line cards), such that each line card is responsible for performing forwarding and packet processing for packets associated with the low-speed ports that line card serves. Thus, as the number of line cards expands, forwarding resources are expanded in at least rough proportion.

The NAS route switch controller, as well as the high-speed ports used to  
15 access the network, are largely relieved of packet processing tasks for traffic passing through the server. The egress port uses a distribution engine that performs the routing lookup for packets received at the high-speed interface, tags the packets with an adjacency table pointer, and sends them to the appropriate forwarding engine for packet processing. The route switch controller updates the routing information  
20 needed by each distribution or forwarding engine, and is largely uninvolved in the processing of individual packets.